**Question: Amdahl’s Law**

Consider the following three processors (X, Y, and Z) that are fabricated on a constant silicon area of 16A. Assume that the single-thread performance of a core increases with the square root of its area.

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Description automatically generated

On each of the three processors, we will execute a workload where S fraction of its work is serial, and where 1-S fraction of its work is infinitely parallelizable. As a function of S, plot the execution time of the workload on each of the three processors. Assume that it takes time T to execute the entire workload using only one of the small cores of Processor Z.

Please label the value of the y-axis intercept and the slope.

1. Processor X

A line with text on it

Description automatically generated

1. Processor Y

A line with text on it

Description automatically generated

1. Processor Z

A line with text on it

Description automatically generated

1. Which processor has the lowest execution time for the widest range of S?
2. Typically, for a realistic workload, the parallel fraction is not infinitely parallelizable. What are the three fundamental reasons?

**Solution: Amdahl’s Law**

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Please label the value of the y-axis intercept and the slope.

1. Processor X

A line with text and numbers

Description automatically generated with medium confidence

1. Processor Y

A graph of slope and a line

Description automatically generated with medium confidence

1. Processor Z

A graph of a slope

Description automatically generated

1. Which processor has the lowest execution time for the widest range of S, what is the major reason for this?

X

1. Typically, for a realistic workload, the parallel fraction is not infinitely parallelizable. What are the three fundamental reasons?

Synchronization

Load imbalance

Resource contention

**Question: Cache Coherence**

You just got back a prototype of your latest processor design, which has two cores and uses the MESI cache coherence protocol for each core’s private L1 caches.

A. **Scenario 1** Let’s say that you discover that there are some bugs in the design of your processor’s coherence modules. Specifically, the BusRead and BusWrite signals on the module occasionally do not get asserted when they should have (but data still gets transferred correctly to the cache). Fill in the table below with a ✔ if, for each MESI state, the missing signal has no effect on correctness. If correctness may be affected, fill in a ✖.

**A group of white squares with black text

Description automatically generated**

B. **Scenario 2** Let’s say that instead you discover that there are no bugs in the design of your processor’s coherence modules. Instead, however, you find that occasionally cosmic rays strike the MESI state storage in your coherence modules, causing a state to instantaneously change to another.

Fill in a cell in the table below with a ✔ if, for a starting MESI state on the top, instantaneously changing the state to the state on the left affects neither correctness nor performance. Fill in a cell in the table with a ○ if correctness is not affected but performance could be affected by the state change. If correctness may be affected, fill in a ✖.

A diagram of a number of squares

Description automatically generated with medium confidence

**Solution: Cache Coherence**

You just got back a prototype of your latest processor design, which has two cores and uses the MESI cache coherence protocol for each core’s private L1 caches.

A. **Scenario 1** Let’s say that you discover that there are some bugs in the design of your processor’s coherence modules. Specifically, the BusRead and BusWrite signals on the module occasionally do not get asserted when they should have (but data still gets transferred correctly to the cache). Fill in the table below with a ✔ if, for each MESI state, the missing signal has no effect on correctness. If correctness may be affected, fill in a ✖.

**A group of black squares with black x marks

Description automatically generated with medium confidence­­­**

B. **Scenario 2** Let’s say that instead you discover that there are no bugs in the design of your processor’s coherence modules. Instead, however, you find that occasionally cosmic rays strike the MESI state storage in your coherence modules, causing a state to instantaneously change to another.

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A diagram of a number of different types of symbols

Description automatically generated with medium confidence